(Pages : 2) **2500**

Reg. No. : .....

Name : .....

Sixth Semester B.Tech. Degree Examination, May 2013
(2008 Scheme)
08.601 : MICROCONTROLLER BASED SYSTEM DESIGN (TA)

Time : 3 Hours Max. Marks : 100

PART – A

Answer **all** questions. **Each** question carries **4** marks.

1. How internal and external program memory is accessed in 8051 ?
2. Explain the format of SCON special function register of 8051.
3. Write a note on multiprocessor communication in 8051.
4. What is an interrupt ? What are the interrupts available in 8051 ? List down their priorities.
5. Give the functions of 8051 pins
   i) $\overline{EA}$
   ii) PSEN
   iii) RESET
6. What is a watchdog timer ? Explain its function.
7. What are the peripheral features in PIC 16F877 controller ?
8. What is pipelining ? What are its advantages ?
9. Mention the data types supported by ARM.
10. What is an exception ? How does it differ from an interrupt ? Explain the differences by reference to ARM processor. **(10×4=40 Marks)**

P.T.O.

PART – B

Answer **any two** questions from **each** Module.

Module – I

11. Write an ALP for 8051 to send 50 output pulses at P2.0. Vary the duration of pulse using NOP.

12. a) Briefly explain the fetch/execute sequences in 8051.

    b) Explain program status word in 8051.

13. a) How are port latch and port pins of 8051 different ? How does 8051 microcontroller interpret that a latch or port pin has to be read ?

    b) There is no 8051 instruction to do only subtraction instead there is SUB B instruction. How to implement subtraction without borrow ?

Module – II

14. Write a program to generate a square wave with $T_1 = 1$ ms and $T_2 = 0.8$ ms.

15. Explain the interfacing of

    a) Stepper motor

    b) LCD module with 8051 microcontroller.

16. Draw the internal architecture of PIC 16F877 and explain.

Module – III

17. Explain clearly various operating modes of ARM processor.

18. Draw a typical ARM core with 3 stage pipeline and explain fetch , decode and execute operation in detail.

19. Write notes on :

    a) Load-store constructions in ARM

    b) Cross assembler. **(6×10=60 Marks)**